UNIVERSITÀ
DEGLI STUDI DI MILANO-BICOCCA

SYLLABUS DEL CORSO

Informatica Industriale

2324-1-F1801Q139

Aims

The course target is giving the knowledge necessary to solve the control and the design of interfaces between external world and internal eleboration unit, analyzing and comparing different hardware and software solutions based on the use of microcontrollers. At the end of the course the students will be able to develop an embedded application using a microcontroller and designing digital logic circuits, debugging them by means of simulations using a specific HDL software
The aim of the course is to provide the skills needed for digital circuits design on programmable hardware. At the end of the course, students will be able to independently develop an embedded application using an FPGA and designing digital logic circuits, performing simulation-level debugging, and using specific software for circuit simulations designed through Hardware Description Languages.

Contents

1 Boole Algebra
2 Combinatory Digital Circuits
3 Sequential Digital Circuits
4 Finite-State-Machine Circuit Design
5 VHDL (Very High Speed Integrated Circuits Descritpion Language) Introduction
6 Combinatory and Sequential Circuits in VHDL
7 Design of Digital Circuits in VHDL
8 FPGA Design

Detailed program

Binary Code
o Introduction and Positional Notation
o Octal and Hexadecimal Code, Hamming Distance
o Binary Arithmetic (sum, difference, product and division)

Logic Operators and Logical Components
o Basic Logical Operators, De Morgan and Consensus theorems
o Combinatory Synthesis by Sum-of-Products or Product-of-Sums
o Karnaugh Maps, Static and Dynamic Hazards

?Combinatory Logic
o Encoder and Decoder, Multiplexer and Demultiplexer, Comparator, Parity Checker and Generator
o Half-Adder and Full-Adder

Sequential Logic
o Latches: D-Latch, SR-Latch
o Flip-Flop: D-Flip-Flop, JK-FLIP-FLOP, T-Flip-Flop
o Registers and Counters
o Exercises
o LTSPICE Exercise

Finite-State-Machines (FSM)
o Mealy and Moore FSM
o Exercises

The VHDL as Hardware Description Languages: an Overview
o Programmable Logic Devices, Dedicated CMOS Design (ASIC)
o VHDL. A simple design example
o Entity Declaration. Architecture Declaration, Assignments, Concurrent Statements
o The Process

Combinatory Logic in VHDL
o Bus Slice and Swap, Basic Logical Operations, Functional Logical Stages
o Decoder, Encoder, Multiplexer, Demultiplexer
o Advanced Functional Logical Stages
o Half-Adder, Full-Adder

VHDL Design Methods
o VHDL Descriptions, Three possible approaches
o Data Flow (key word ‘<=’), Sequential (key word ‘process’), Structural (key word ‘component’)
o Signals and Variables
o Exercise 1 – Full-adder
o Exercise 2 – Binary-BCD Converter

Memory Components
o Latch D, SR
o Flip-Flop D, JK, T
o Master-slave
o Registers (PIPO, SIPO, SISO)
o Exercise 3 – Latch e Flip-flop
o Exercise 4 – Registers in VHDL
o Exercise 5 – Counters Design in VHDL
A Design Example of a FSM in VHDL

Serial Interfaces (I2C and SPI)

Lab Exercise with Opal-Kelly XEM6010 (Xilinx® Spartan 6 FPGA)

Prerequisites

?C Programming, machine-level programming (I / O management and interrups).

Teaching form

Lectures for basic concepts. Classroom exercises with the presentation and discussion of digital circuits in VHDL/Verilog. Laboratory activity for the development of digital circuits and for the use of FPGAs in simple applications
The course will be held in Italian.

In the Covid-19 emergency period, the lessons will take place completely remotely synchronously (webconference) with some physical presence events.

The video recording of the lesson will then be immediately online on the elearning platform.

Textbook and teaching resource

- Notes and slides
- “Circuit Design with VHDL” Volnei A. Pedroni MIT Press

Semester

Second Semester

Assessment method

The final exam is oral and it is divided into two parts.

The score assigned to each part is 15/30 each.
In the first part the student will present documentation and functionalities of a specific hardware system developed entirely by the same student and related to a project topic assigned in class to groups consisting of at most two students.
In the second part, the examination of the student will take place through two questions related to the topics covered during the course, and in particular the first one concerning the combinatory circuits and a second on the sequential circuits.

Office hours

Monday 10-12

Sustainable Development Goals

INDUSTRY, INNOVATION AND INFRASTRUCTURE