UNIVERSITÀ
DEGLI STUDI DI MILANO-BICOCCA

SYLLABUS DEL CORSO

Informatica Industriale

2425-1-F1801Q139

Aims

The course aims to provide the skills necessary to solve the problems of digital circuits design on programmable hardware. At the end of the course, students will be able to independently develop an embedded application using a programmable logic device (FPGA) and designing digital logic circuits, debugging them at the simulation level and using specific tools of Computer Aided Design (CAD) for the simulation of digital circuits designed through Hardware Description Languages.

Contents

1 Boole Algebra
2 Combinatory Digital Circuits
3 Sequential Digital Circuits
4 Finite-State-Machine Digital Circuit Design
5 Introduction to VHDL (Very High Speed Integrated Circuits Descritpion Language) Introduction
6 Combinatory and Sequential Circuits in VHDL
7 Design of Digital Circuits in VHDL
8 FPGA Design

Detailed program

Binary Code
o Introduction and Positional Notation
o Octal and Hexadecimal Code, Hamming Distance
o Binary Arithmetic (sum, difference, product and division)

Logic Operators and Logical Components
o Basic Logical Operators, De Morgan and Consensus theorems
o Combinatory Synthesis by Sum-of-Products or Product-of-Sums
o Karnaugh Maps, Static and Dynamic Hazards

?Combinatory Logic
o Encoder and Decoder, Multiplexer and Demultiplexer, Comparator, Parity Checker and Generator
o Half-Adder and Full-Adder

Sequential Logic
o Latches: D-Latch, SR-Latch
o Flip-Flop: D-Flip-Flop, JK-FLIP-FLOP, T-Flip-Flop
o Registers and Counters
o Exercises
o LTSPICE Exercise

Finite-State-Machines (FSM)
o Mealy and Moore FSM
o Exercises

The VHDL as Hardware Description Languages: an Overview
o Programmable Logic Devices, Dedicated CMOS Design (ASIC)
o VHDL. A simple design example
o Entity Declaration. Architecture Declaration, Assignments, Concurrent Statements
o The Process

Combinatory Logic in VHDL
o Bus Slice and Swap, Basic Logical Operations, Functional Logical Stages
o Decoder, Encoder, Multiplexer, Demultiplexer
o Advanced Functional Logical Stages
o Half-Adder, Full-Adder

VHDL Design Methods
o VHDL Descriptions, Three possible approaches
o Data Flow (key word ‘<=’), Sequential (key word ‘process’), Structural (key word ‘component’)
o Signals and Variables
o Exercise 1 – Full-adder
o Exercise 2 – Binary-BCD Converter

Memory Components
o Latch D, SR
o Flip-Flop D, JK, T
o Master-slave
o Registers (PIPO, SIPO, SISO)
o Exercise 3 – Latch e Flip-flop
o Exercise 4 – Registers in VHDL
o Exercise 5 – Counters Design in VHDL
A Design Example of a FSM in VHDL

Serial Interfaces (I2C and SPI)

Lab Exercise with Opal-Kelly XEM6010 (Xilinx® Spartan 6 FPGA)

Prerequisites

?C Programming, machine-level programming (I / O management and interrups).

Teaching form

The planned activities are:

- 27 hours of LECTURES in delivery mode, in which the fundamental concepts of digital logic design will be presented.
- 12 hours of EXERCISES in delivery mode, in the classroom with presentation and discussion of examples of digital circuits described in VHDL/Verilog.
- 9 hours of GROUP WORK in interactive mode, for development and simulation of components and use of FPGAs in simple applications.

Attendance is strongly recommended and is essential for all activities.

The course will be delivered in Italian.

Textbook and teaching resource

- Notes and slides
- "Introduction to digital systems design". Donzellini, Giuliano, Luca Oneto, Domenico Ponta, and Davide Anguita. Cham: Springer, 2019.
- “Circuit Design with VHDL” Volnei A. Pedroni MIT Press

Semester

Second Semester

Assessment method

The exam consists of a WRITTEN TEST and an ORAL TEST.

The WRITTEN TEST consists of THREE QUESTIONS:
Question 1 requires studying and/or synthesizing simple combinatorial networks.
Question 2 focuses on the synthesis of simple sequential networks.
Question 3 is based on the synthesis of mixed digital systems (with combinatorial components and sequential components).

The skills and knowledge required to pass the written test are:
QUESTION 1

- Boolean algebra, logical operators and basic logical components;
- synthesis of circuits via Karnaugh map and/or Sums of Products (Products of Sums);
  QUESTION 2
- basic schematics of memory elements and sequential logic;
  QUESTION 3
- Finite State Machines and Sequential Digital Circuits

The evaluation CRITERIA for the written test are:

- formal and analytical correctness of the logical circuits solution of the proposed questions;
- the level of synthesis and clarity of exposition of the logic circuits.

The ORAL EXAM will be characterized by two phases:

- Interview to discuss the written test;
- Interview on the Report on GROUP WORK for the development of components and the use of FPGAs in simple applications.

Skills and evaluation criteria of the oral test are based on the ability to critically discuss the written test (for example correctly commenting on the circuit choices in response to the questions and proposing further interpretations of these solutions).

Office hours

Monday 10-12

Sustainable Development Goals

INDUSTRY, INNOVATION AND INFRASTRUCTURE