UNIVERSITÀ
DEGLI STUDI DI MILANO-BICOCCA

SYLLABUS DEL CORSO

Informatica Industriale

2627-1-F1802Q126

Aims

The course aims to provide students with the fundamental knowledge and skills required for the analysis, design, and verification of digital logic systems using Hardware Description Languages (HDLs) and Field-Programmable Gate Arrays (FPGAs). Particular emphasis is placed on the use of professional Computer-Aided Design (CAD) tools for the simulation, synthesis, and verification of digital circuits, together with an introduction to the design flow of digital integrated circuits (ASICs).

Upon successful completion of the course, students will be able to design simple digital systems, describe them using VHDL, verify their functionality through simulation, implement them on FPGA devices, and use CAD tools for the design of silicon-based digital integrated circuits.

Expected learning outcomes

- Knowledge and understanding
  Students will acquire the fundamental knowledge of digital logic system design, programmable logic devices (FPGAs), Hardware Description Languages (VHDL), and the operating principles of Computer-Aided Design (CAD) tools for the design, simulation, and verification of digital circuits and integrated circuits.

- Applying knowledge and understanding
  Students will be able to analyze, design, and simulate combinational and sequential digital circuits, describe them using VHDL, implement them on FPGA devices, and use CAD tools for the design and verification of basic digital systems and integrated circuits.

- Making judgements
  Students will develop the ability to evaluate alternative design solutions for simple digital systems, critically interpret simulation and debugging results, and select appropriate design solutions according to given specifications.

- Communication skills

Students will be able to describe the operation of digital systems, justify their design choices, and effectively present the results of design and simulation activities using appropriate scientific and technical terminology.

- Learning skills
  Students will acquire the methodological skills required for independent learning in digital system design, the use of CAD tools and Hardware Description Languages, and for undertaking more advanced studies in digital system design, FPGA-based systems, and digital integrated circuit (ASIC) design.

Contents

1. Number systems and binary codes.
2. Boolean algebra and logic circuit synthesis.
3. Combinational logic circuits.
4. Sequential logic circuits.
5. Finite State Machines (FSMs).
6. VHDL Hardware Description Language.
7. Design, simulation, and verification of digital systems using VHDL.
8. Programmable logic devices (FPGAs) and digital interfaces (SPI and I²C).
9. Digital signal acquisition and processing on FPGAs in the presence of noise.
10. Introduction to digital integrated circuit (ASIC) design using Computer-Aided Design (CAD) tools.

Detailed program

1. Number Systems and Binary Codes

- Introduction to number systems
- Binary representation of numbers
- Octal and hexadecimal number systems
- Gray code
- Hamming distance
- Binary arithmetic

2. Boolean Algebra

- Basic logic operators
- De Morgan's theorems
- Consensus theorem
- Sum-of-Products (SOP) synthesis
- Product-of-Sums (POS) synthesis
- Logic minimization using Karnaugh maps
- Static and dynamic hazards

3. Combinational Logic Circuits

- Logic gates
- Encoders, decoders, multiplexers, and demultiplexers
- Comparators
- Parity generators and parity checkers

- Half-adders and full-adders

4. Sequential Logic Circuits

- SR and D latches
- D, JK, and T flip-flops
- Registers
- Counters

5. Finite State Machines (FSMs)

- Mealy model
- Moore model
- Design methodologies
- Design examples

6. Hardware Description Languages

- Programmable logic devices
- FPGAs and ASICs
- Introduction to VHDL
- Entity
- Architecture
- Data types
- Signals and variables
- Concurrent statements
- Processes

7. Digital Design Using VHDL

- Combinational, sequential, and structural modeling
- Reusable components
- Buses and vectors
- Logic operators
- Combinational circuit design
- Registers and counters
- Finite State Machine design

8. Digital Interfaces

- SPI
- I^2C

9. Digital Signal Processing on FPGAs

- Digital signal acquisition
- Noise in the digital domain
- Digital filtering techniques
- Signal conditioning
- Implementation on Xilinx® Spartan-7 FPGAs

10. Introduction to Digital Integrated Circuit Design

- ASIC design flow using CAD tools
- Functional simulation

- Logic synthesis
- Timing analysis
- Introduction to digital layout design

Prerequisites

?C Programming, machine-level programming (I / O management and interrups).

Teaching form

The course consists of:

1. 27 hours of lectures, covering the theoretical foundations of digital system design.
2. 6 hours of practical exercises, devoted to design examples and circuit simulation using VHDL and Computer-Aided Design (CAD) tools.
3. 15 hours of group project activities, conducted in an interactive format with the instructor, aimed at:

- developing and simulating digital components using VHDL;
- implementing simple applications on FPGA devices;
- introducing the CAD-based design flow for digital integrated circuits.

Attendance is strongly recommended, particularly for the project activities.

The course is normally taught in Italian. Upon request by one or more students, it may also be delivered in English.

Textbook and teaching resource

- Notes and slides
- "Introduction to digital systems design". Donzellini, Giuliano, Luca Oneto, Domenico Ponta, and Davide Anguita. Cham: Springer, 2019.
- “Circuit Design with VHDL” Volnei A. Pedroni MIT Press

Semester

Second Semester

Assessment method

The assessment consists of a written examination and an oral examination.

Written examination

- The written examination consists of three digital logic design problems.
- The first problem focuses on the analysis and synthesis of combinational logic circuits.
- The second problem concerns the analysis and design of sequential logic circuits.
- The third problem involves the design of simple digital systems combining combinational logic, sequential logic, and finite state machines (FSMs).

The written examination is assessed based on:

- the technical correctness of the proposed solutions;
- the ability to synthesize effective design solutions;
- the clarity and organization of the presented work.

Oral examination:
The oral examination consists of:

- a critical discussion of the written examination;
- the presentation and discussion of the group project developed during the course.

The oral examination assesses:

- the student's understanding of the theoretical concepts;
- the ability to justify design choices;
- the correct use of scientific and technical terminology;
- the ability to critically interpret the results obtained through simulation and FPGA implementation.

Office hours

Monday 10-12

Sustainable Development Goals

INDUSTRY, INNOVATION AND INFRASTRUCTURE