Exercise: Fully Associative Cache: how many (total) Misses?

Using **byte addresses** in this exercise!

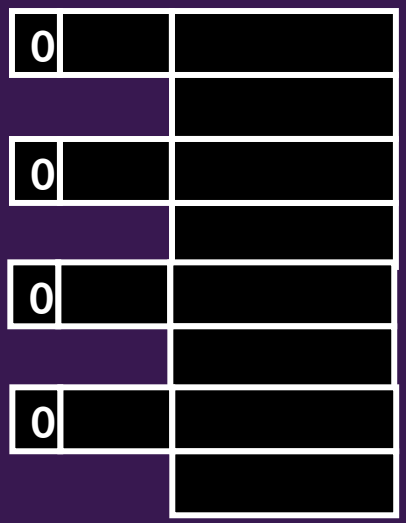
Processor

cache ← M[508]
cache ← M[1016]
cache ← M[504]
cache ← M[24]
cache ← M[540]

Cache

4 blocks in cache
2 words per block

8 byte-addr.s per block

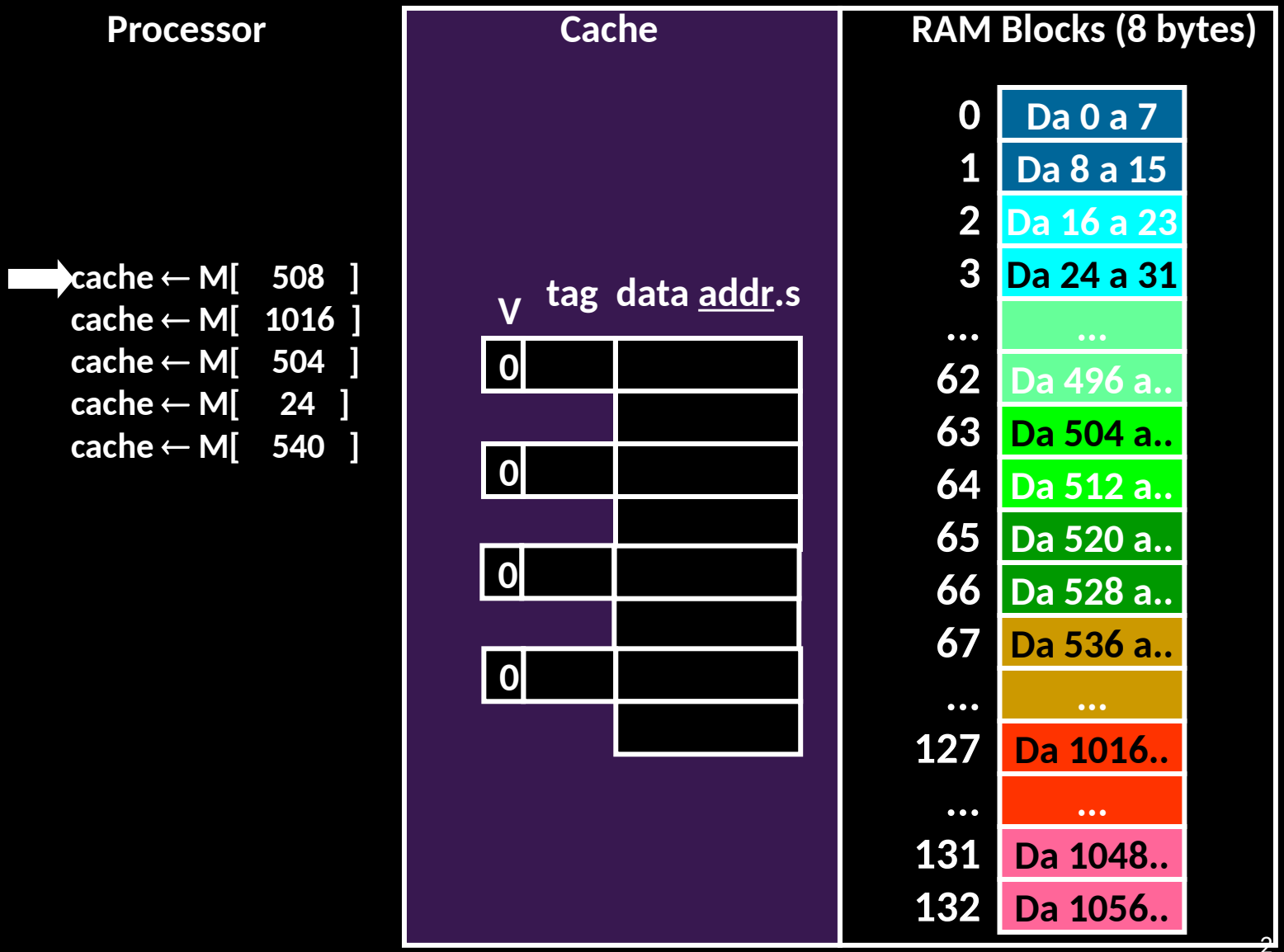


RAM Blocks (8 bytes)

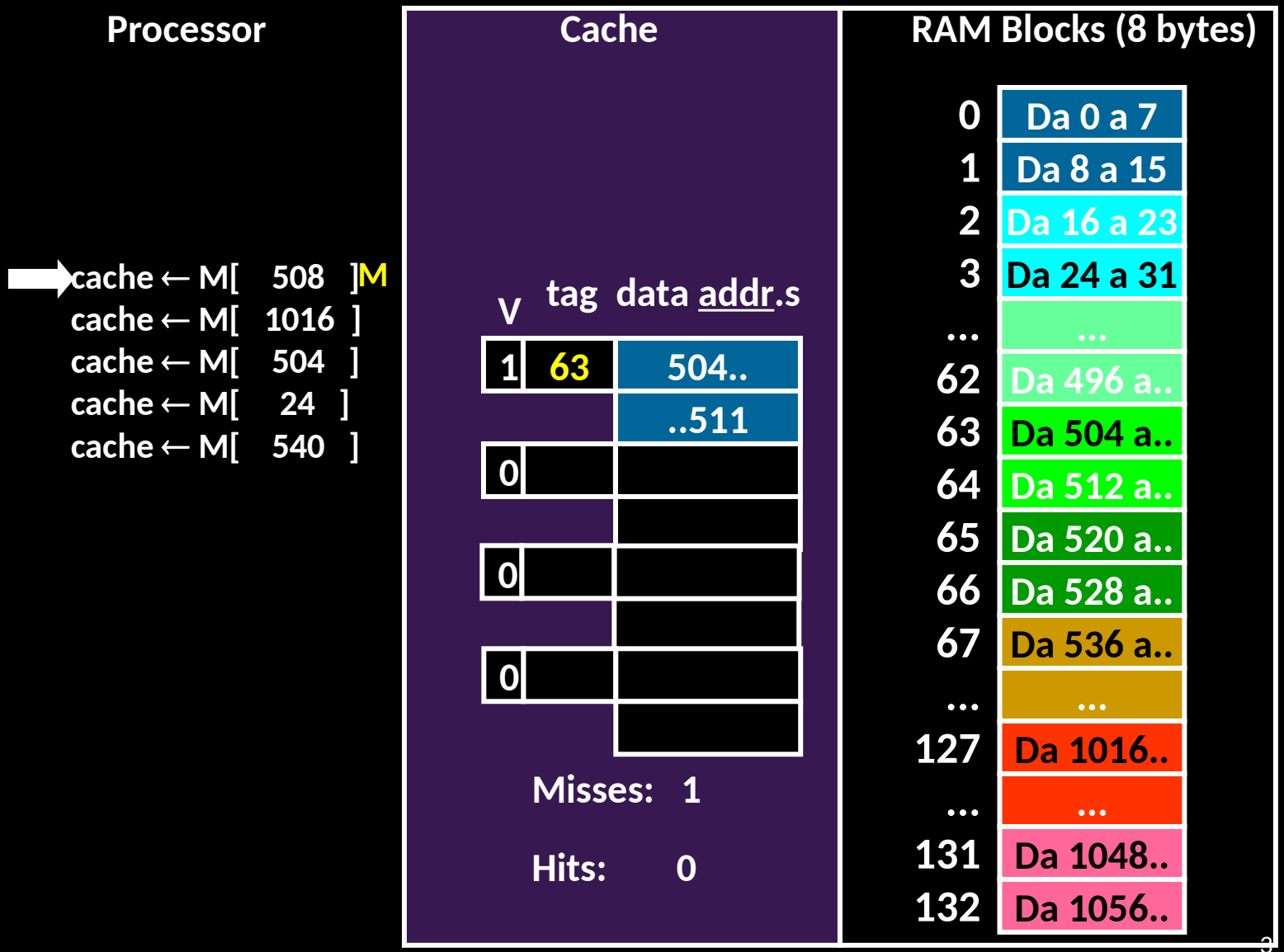
0	Da 0 a 7
1	Da 8 a 15
2	Da 16 a 23
3	Da 24 a 31
…	…
62	Da 496 a..
63	Da 504 a..
64	Da 512 a..
65	Da 520 a..
66	Da 528 a..
67	Da 536 a..
…	…
127	Da 1016..
…	…
131	Da 1048..
132	Da 1056..

1st Access

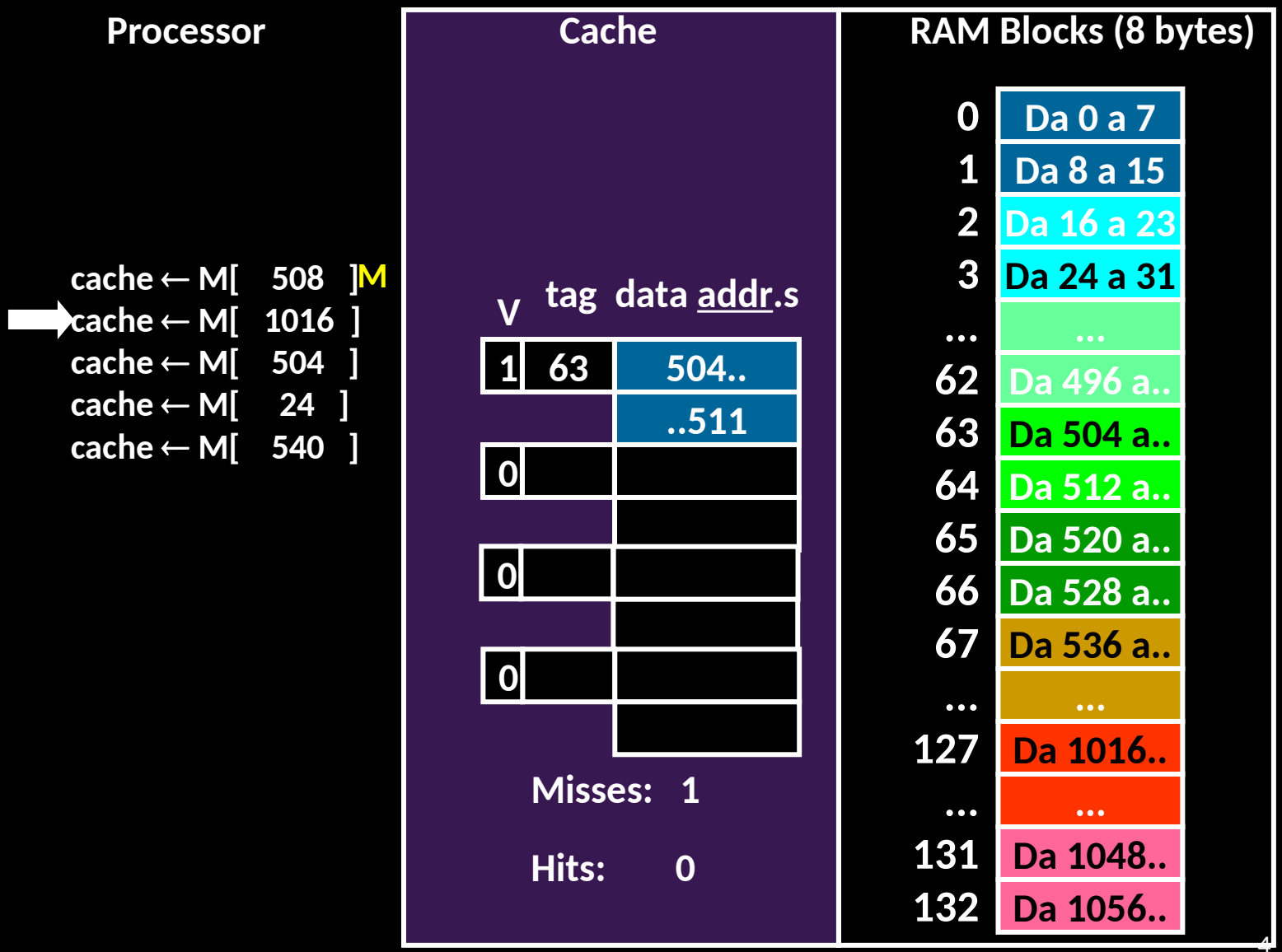
Using RAM block number as tag (and: fully assoc.=>no index)



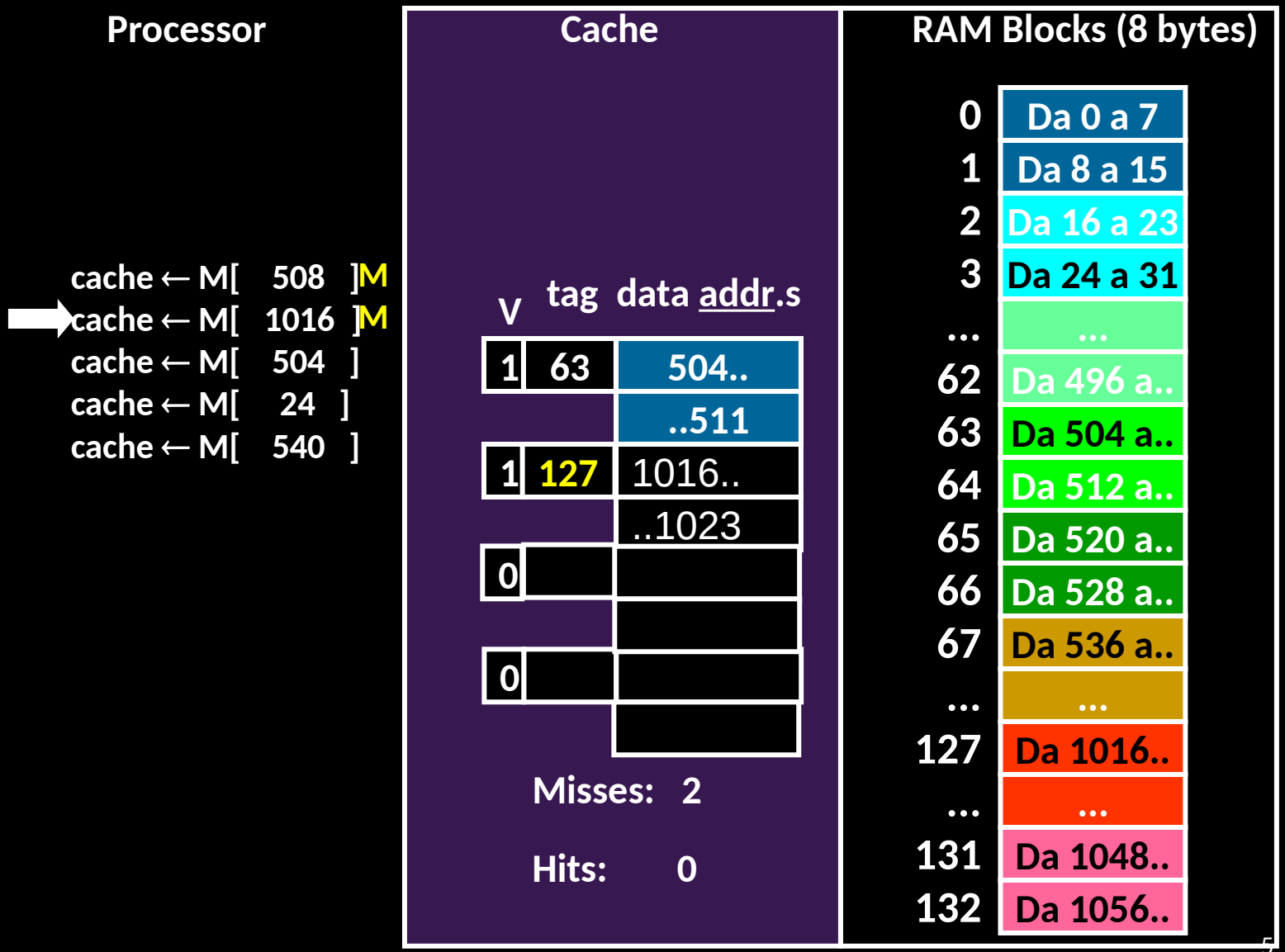
1st Access


Processor
cache ← M[508]M
cache ← M[1016]
cache ← M[504]
cache ← M[24]
cache ← M[540]
Cache
V tag data addr.s
1 63 504..
..511
0
0
0
Misses: 1
Hits: 0
RAM Blocks (8 bytes)
0 Da 0 a 7
1 Da 8 a 15
2 Da 16 a 23
3 Da 24 a 31
... ...
62 Da 496 a..
63 Da 504 a..
64 Da 512 a..
65 Da 520 a..
66 Da 528 a..
67 Da 536 a..
... ...
127 Da 1016..
... ...
131 Da 1048..
132 Da 1056..

2nd Access

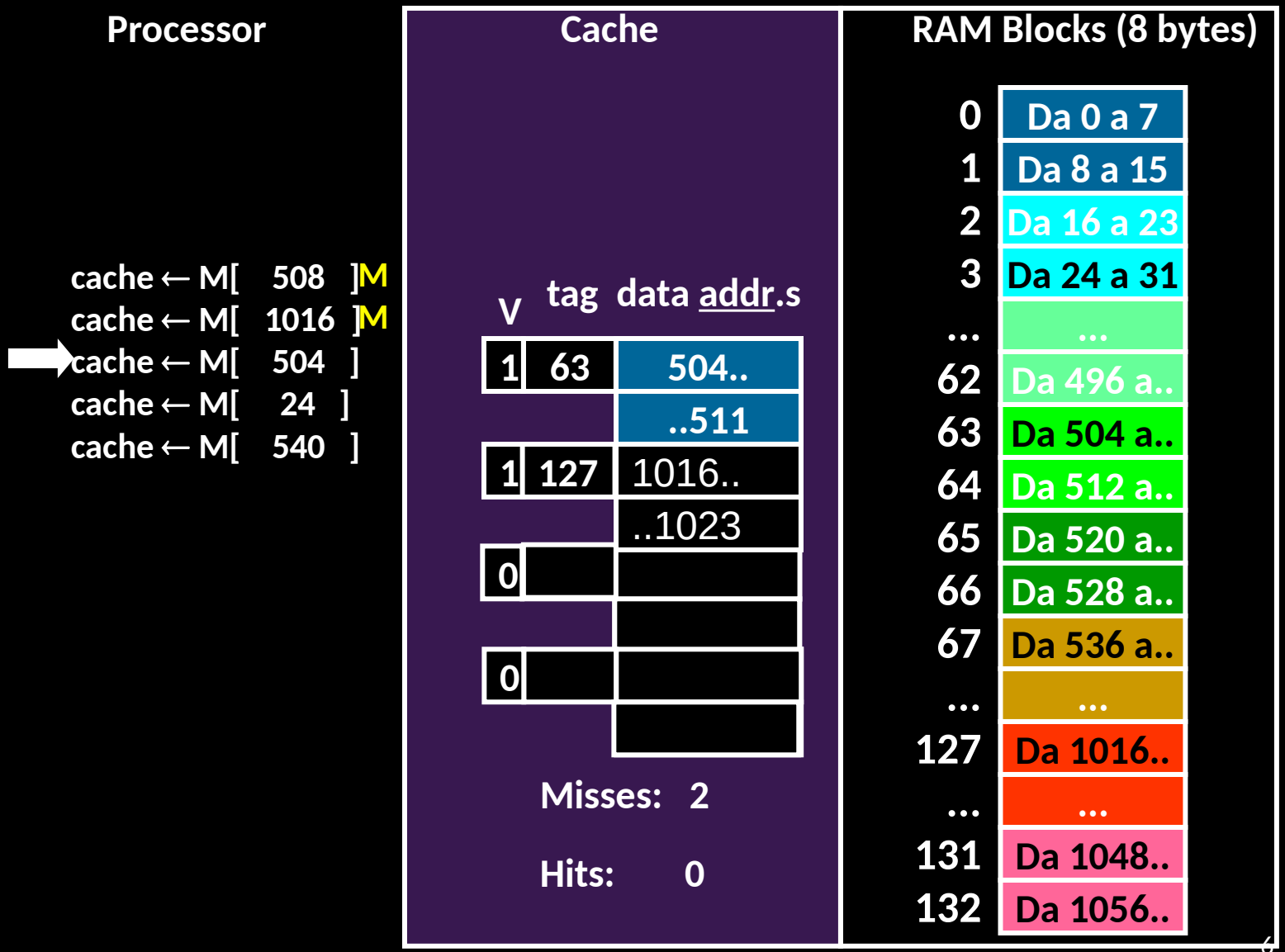

Processor
cache ← M[508]M
cache ← M[1016]
cache ← M[504]
cache ← M[24]
cache ← M[540]
Cache
V
tag
data
addr.s
1
63
504..
..511
0
0
0
Misses: 1
Hits: 0
RAM Blocks (8 bytes)
0 Da 0 a 7
1 Da 8 a 15
2 Da 16 a 23
3 Da 24 a 31
... ...
62 Da 496 a..
63 Da 504 a..
64 Da 512 a..
65 Da 520 a..
66 Da 528 a..
67 Da 536 a..
... ...
127 Da 1016..
... ...
131 Da 1048..
132 Da 1056..

2nd Access

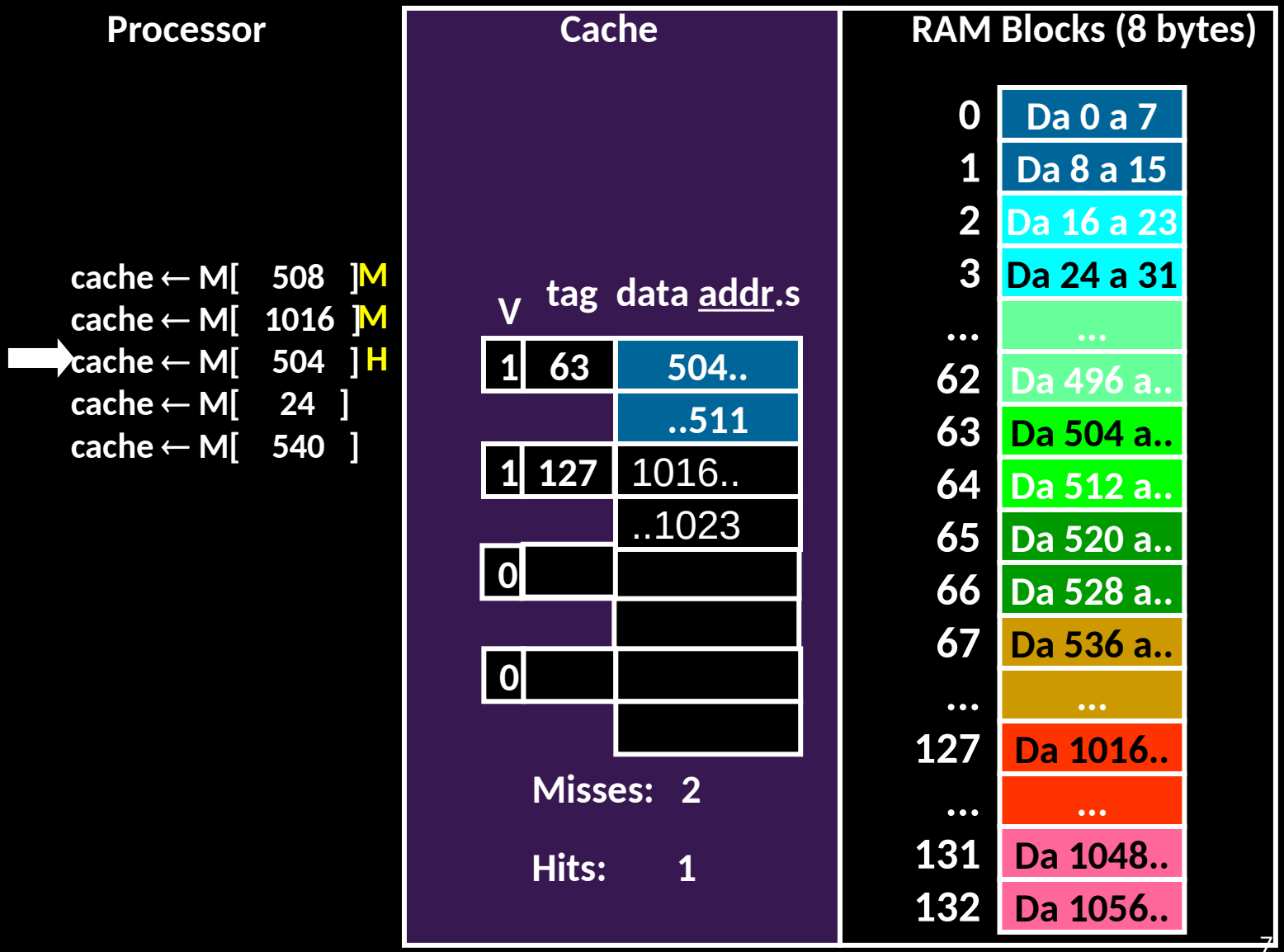

Processor
cache ← M[508]M
cache ← M[1016]M
cache ← M[504]
cache ← M[24]
cache ← M[540]
Cache
V tag data addr.s
1 63 504..
..511
1 127 1016..
..1023
0
0
Misses: 2
Hits: 0
RAM Blocks (8 bytes)
0 Da 0 a 7
1 Da 8 a 15
2 Da 16 a 23
3 Da 24 a 31
... ...
62 Da 496 a..
63 Da 504 a..
64 Da 512 a..
65 Da 520 a..
66 Da 528 a..
67 Da 536 a..
... ...
127 Da 1016..
... ...
131 Da 1048..
132 Da 1056..

3rd Access

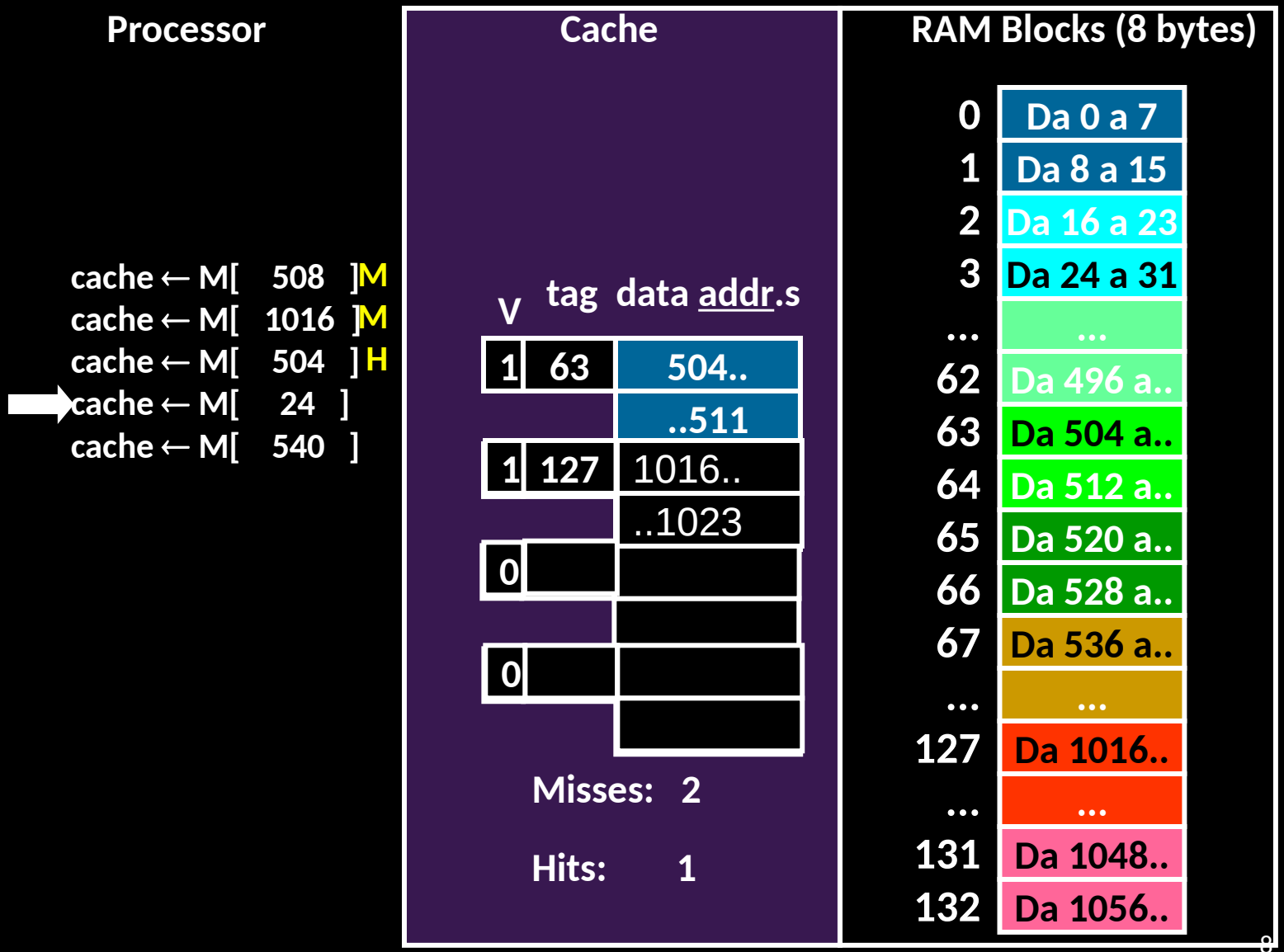
Byte 504 is in a block **already in cache**! (block 63 in RAM, block 0 in cache)



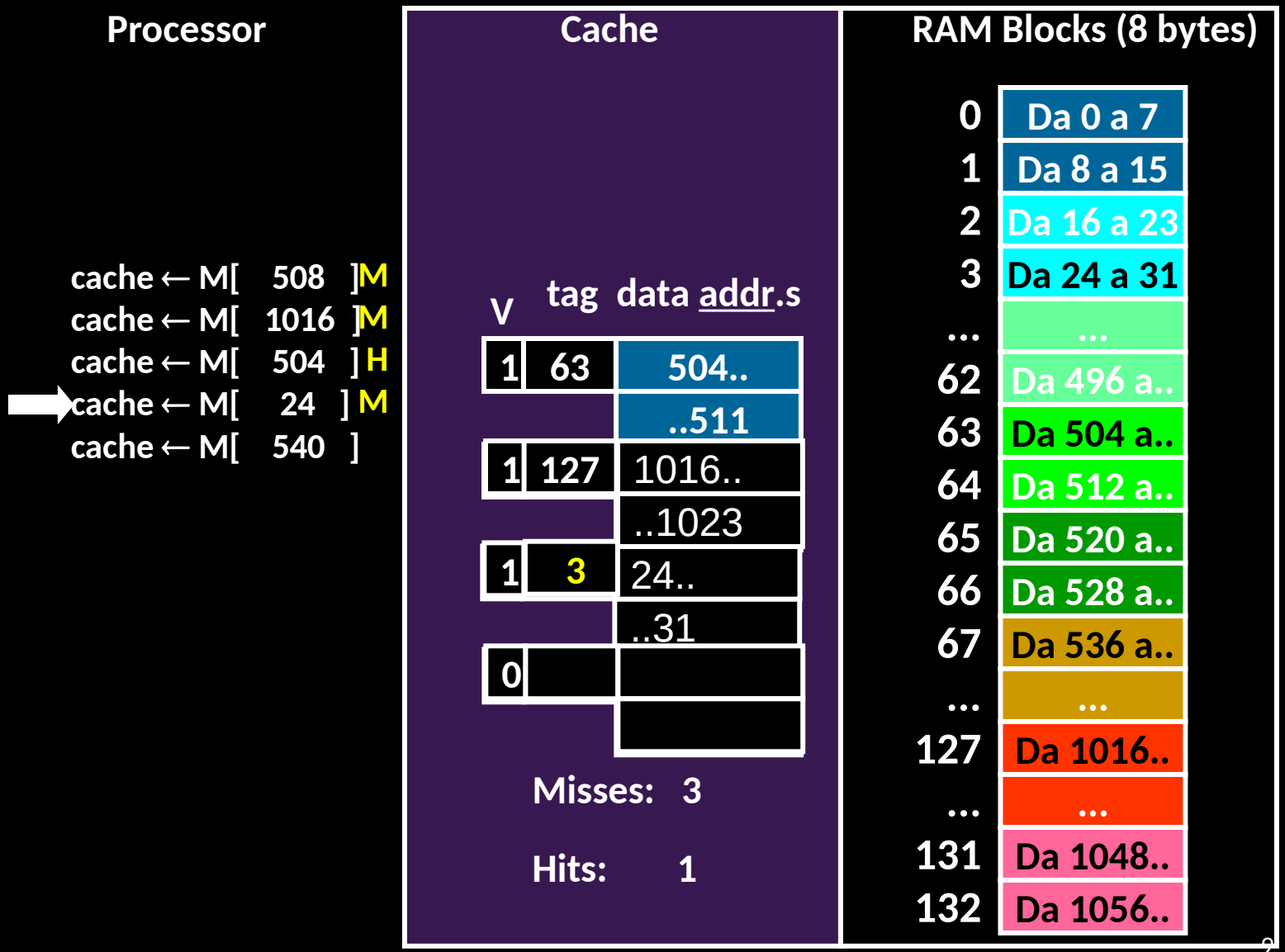
3rd Access


Processor
cache ← M[508]M
cache ← M[1016]M
cache ← M[504] H
cache ← M[24]
cache ← M[540]
Cache
V tag data addr.s
1 63 504..
..511
1 127 1016..
..1023
0
0
Misses: 2
Hits: 1
RAM Blocks (8 bytes)
0 Da 0 a 7
1 Da 8 a 15
2 Da 16 a 23
3 Da 24 a 31
... ...
62 Da 496 a..
63 Da 504 a..
64 Da 512 a..
65 Da 520 a..
66 Da 528 a..
67 Da 536 a..
... ...
127 Da 1016..
... ...
131 Da 1048..
132 Da 1056..

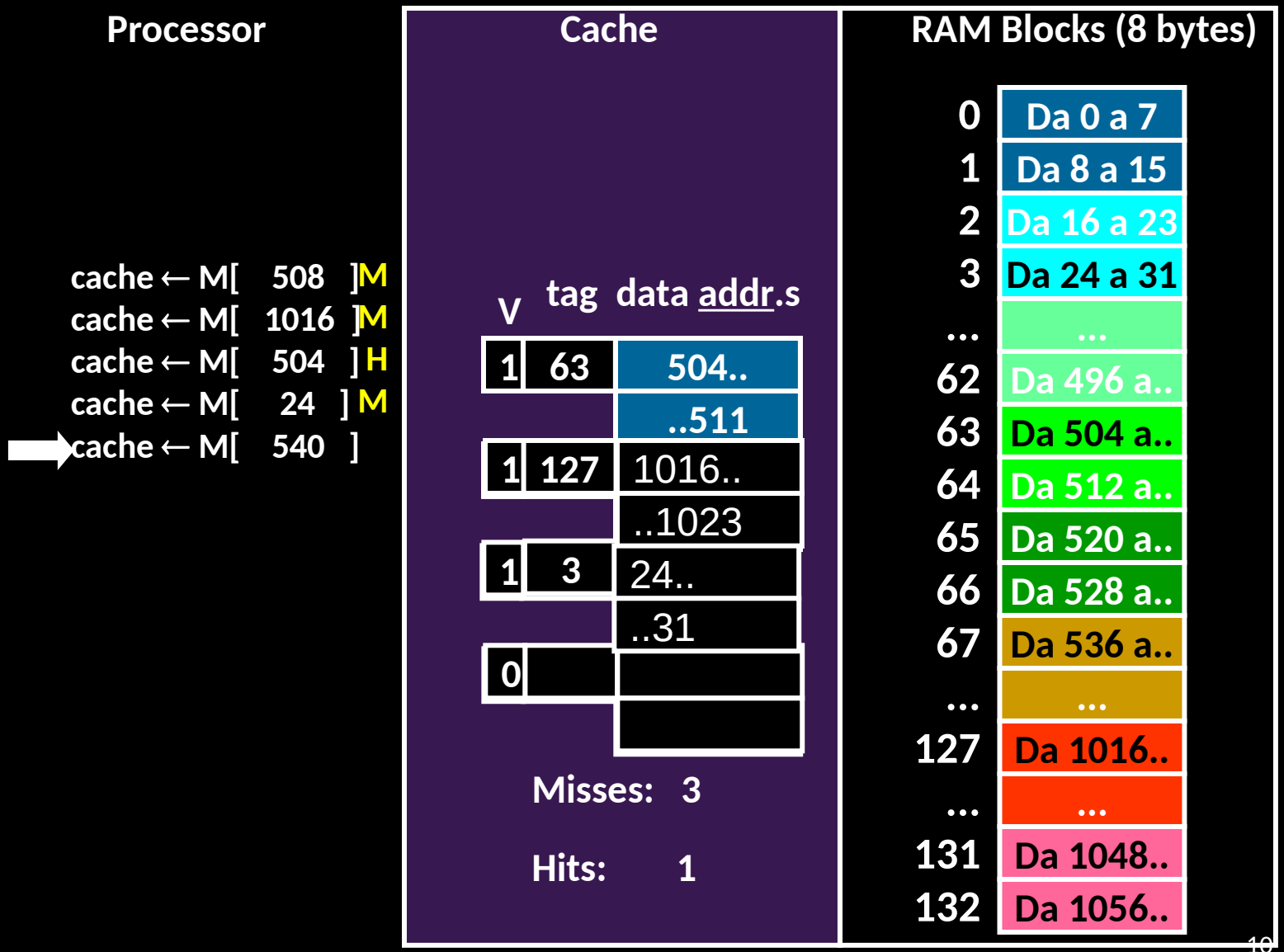
4th Access


Processor
cache ← M[508]M
cache ← M[1016]M
cache ← M[504] H
cache ← M[24]
cache ← M[540]
Cache
V tag data addr.s
1 63 504..
..511
1 127 1016..
..1023
0
0
Misses: 2
Hits: 1
RAM Blocks (8 bytes)
0 Da 0 a 7
1 Da 8 a 15
2 Da 16 a 23
3 Da 24 a 31
... ...
62 Da 496 a..
63 Da 504 a..
64 Da 512 a..
65 Da 520 a..
66 Da 528 a..
67 Da 536 a..
... ...
127 Da 1016..
... ...
131 Da 1048..
132 Da 1056..

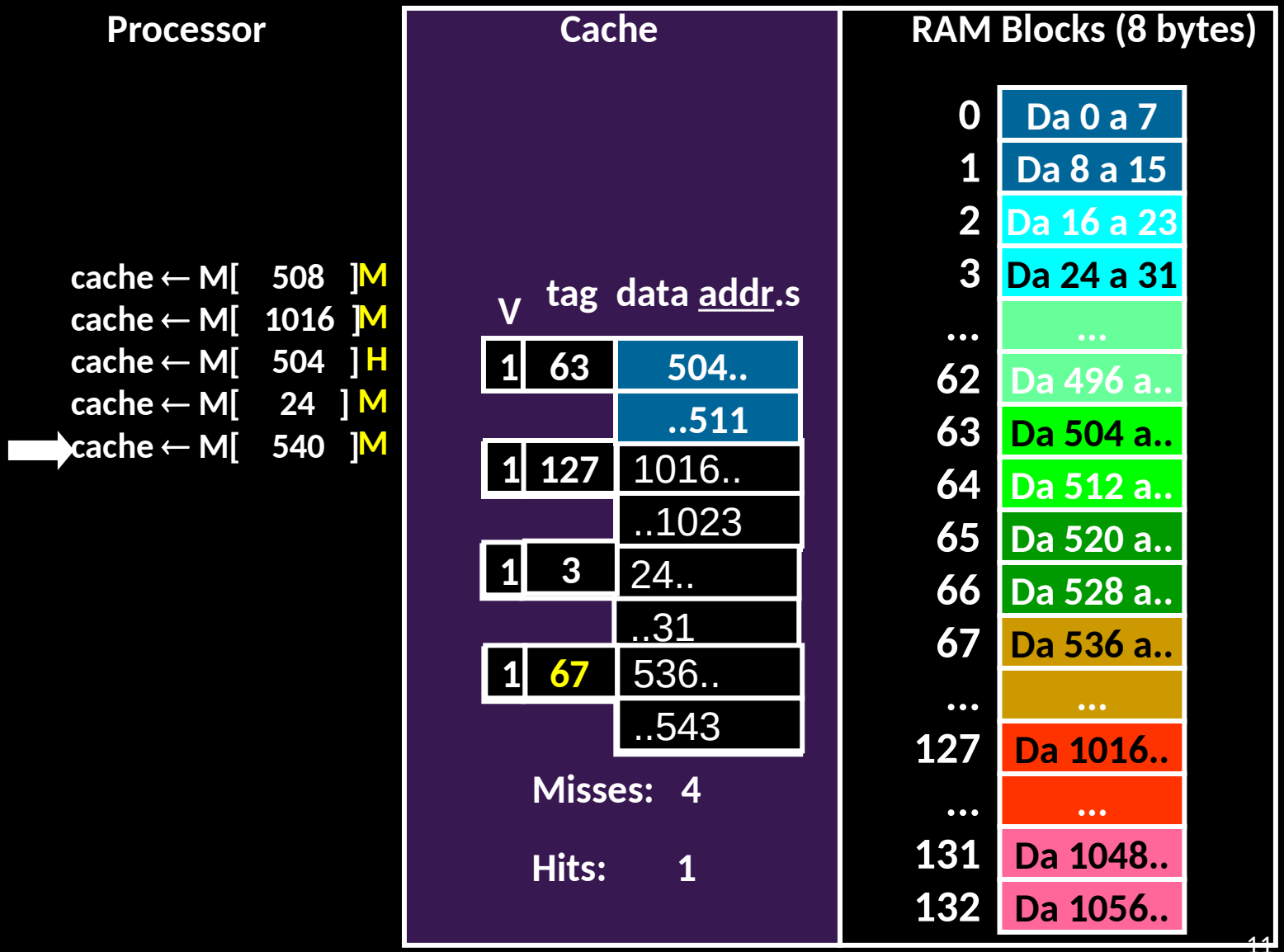
4th Access


Processor
cache ← M[508]M
cache ← M[1016]M
cache ← M[504] H
cache ← M[24] M
cache ← M[540]
Cache
V tag data addr.s
1 63 504..
..511
1 127 1016..
..1023
1 3 24..
..31
0
Misses: 3
Hits: 1
RAM Blocks (8 bytes)
0 Da 0 a 7
1 Da 8 a 15
2 Da 16 a 23
3 Da 24 a 31
... ...
62 Da 496 a..
63 Da 504 a..
64 Da 512 a..
65 Da 520 a..
66 Da 528 a..
67 Da 536 a..
... ...
127 Da 1016..
... ...
131 Da 1048..
132 Da 1056..

5th Access

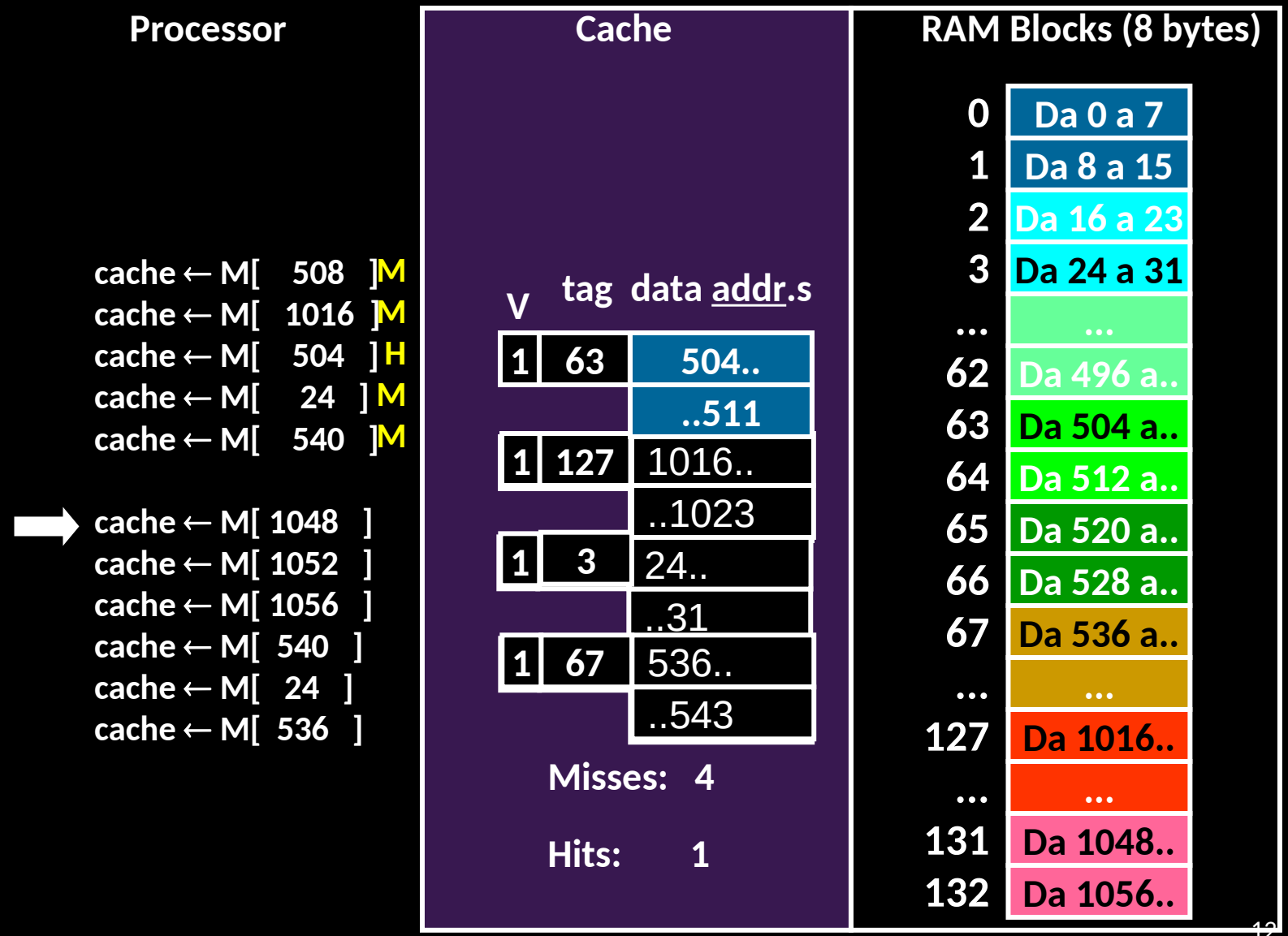

Processor
cache ← M[508] M
cache ← M[1016] M
cache ← M[504] H
cache ← M[24] M
cache ← M[540]
Cache
V tag data addr.s
1 63 504..
..511
1 127 1016..
..1023
1 3 24..
..31
0
Misses: 3
Hits: 1
RAM Blocks (8 bytes)
0 Da 0 a 7
1 Da 8 a 15
2 Da 16 a 23
3 Da 24 a 31
... ...
62 Da 496 a..
63 Da 504 a..
64 Da 512 a..
65 Da 520 a..
66 Da 528 a..
67 Da 536 a..
... ...
127 Da 1016..
... ...
131 Da 1048..
132 Da 1056..

5th Access


Processor
cache ← M[508]M
cache ← M[1016]M
cache ← M[504] H
cache ← M[24] M
cache ← M[540]M
Cache
V tag data addr.s
1 63 504..
..511
1 127 1016..
..1023
1 3 24..
..31
1 67 536..
..543
Misses: 4
Hits: 1
RAM Blocks (8 bytes)
0 Da 0 a 7
1 Da 8 a 15
2 Da 16 a 23
3 Da 24 a 31
... ...
62 Da 496 a..
63 Da 504 a..
64 Da 512 a..
65 Da 520 a..
66 Da 528 a..
67 Da 536 a..
... ...
127 Da 1016..
... ...
131 Da 1048..
132 Da 1056..

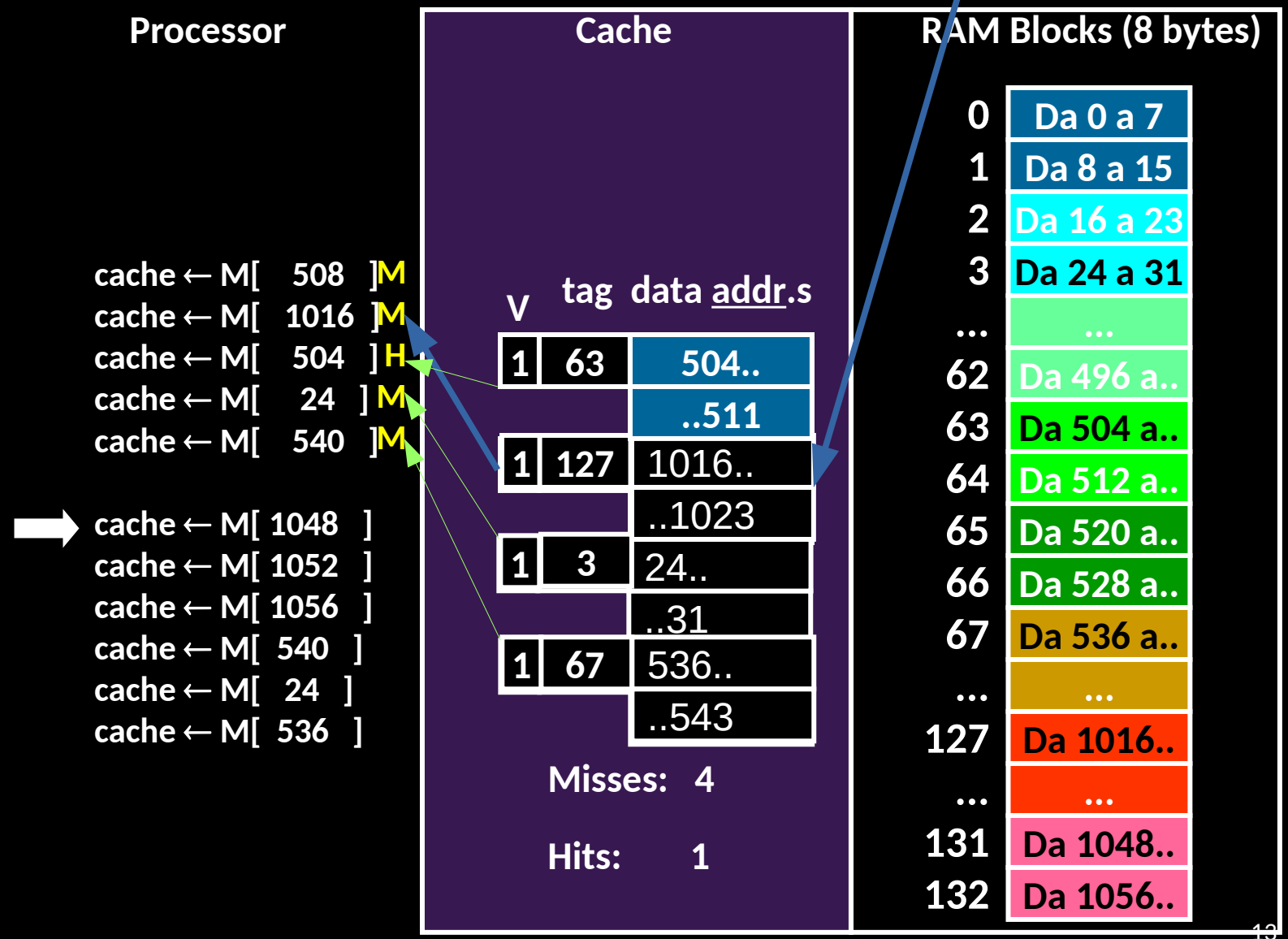
First use of LRU

Cache full, byte's block missing => replace based on LRU

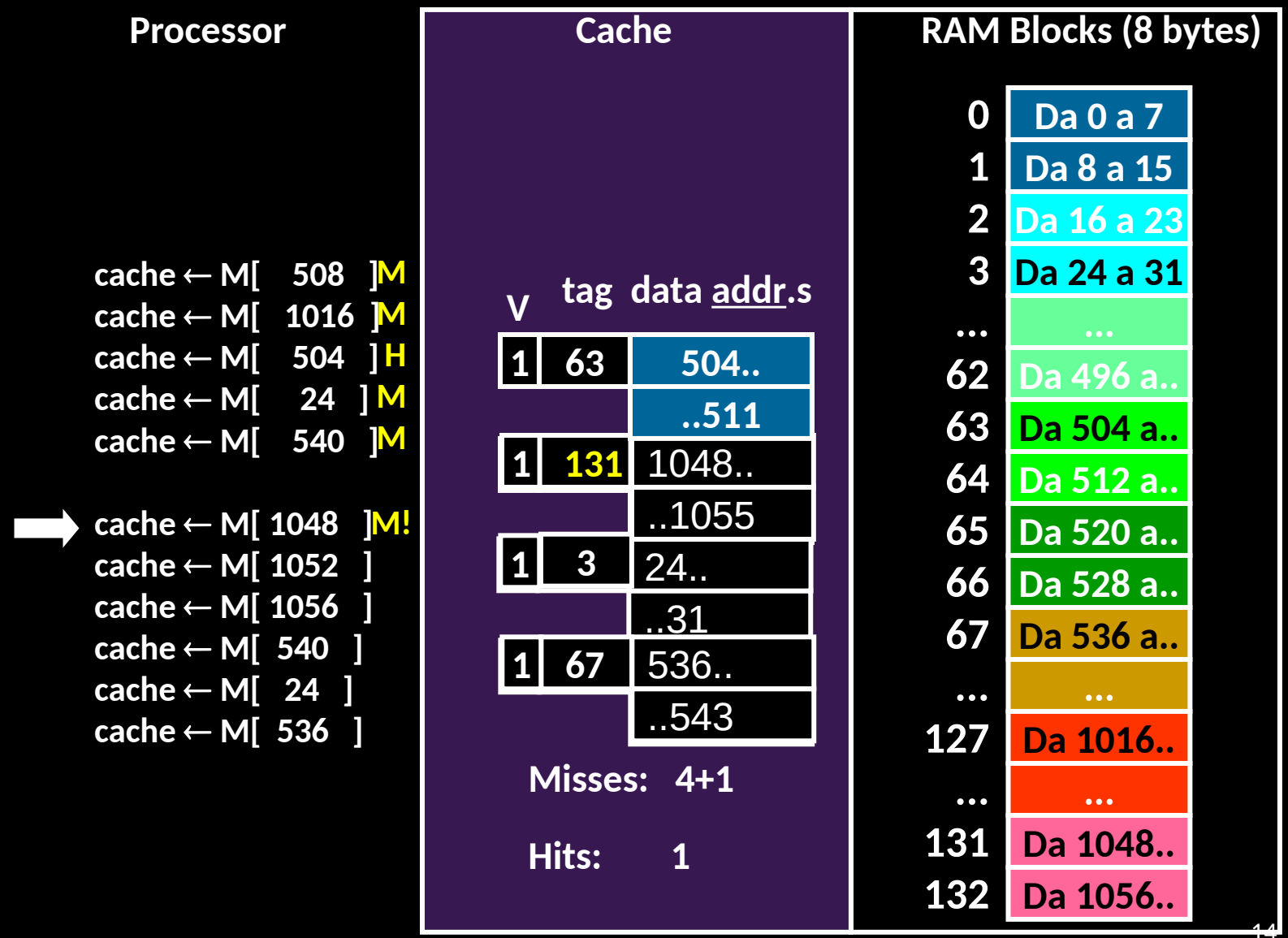


...

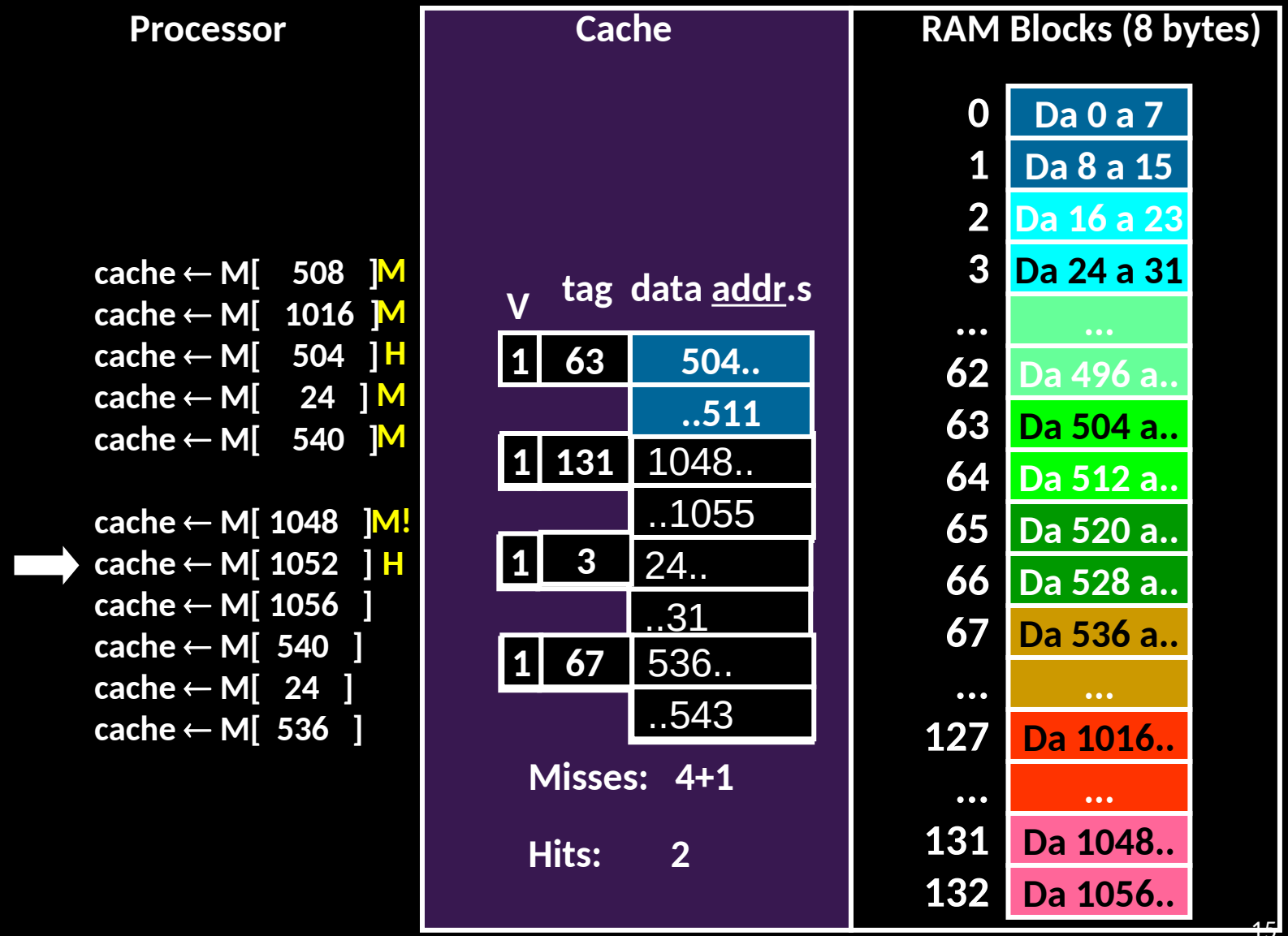
Least recently used block in cache is:



...

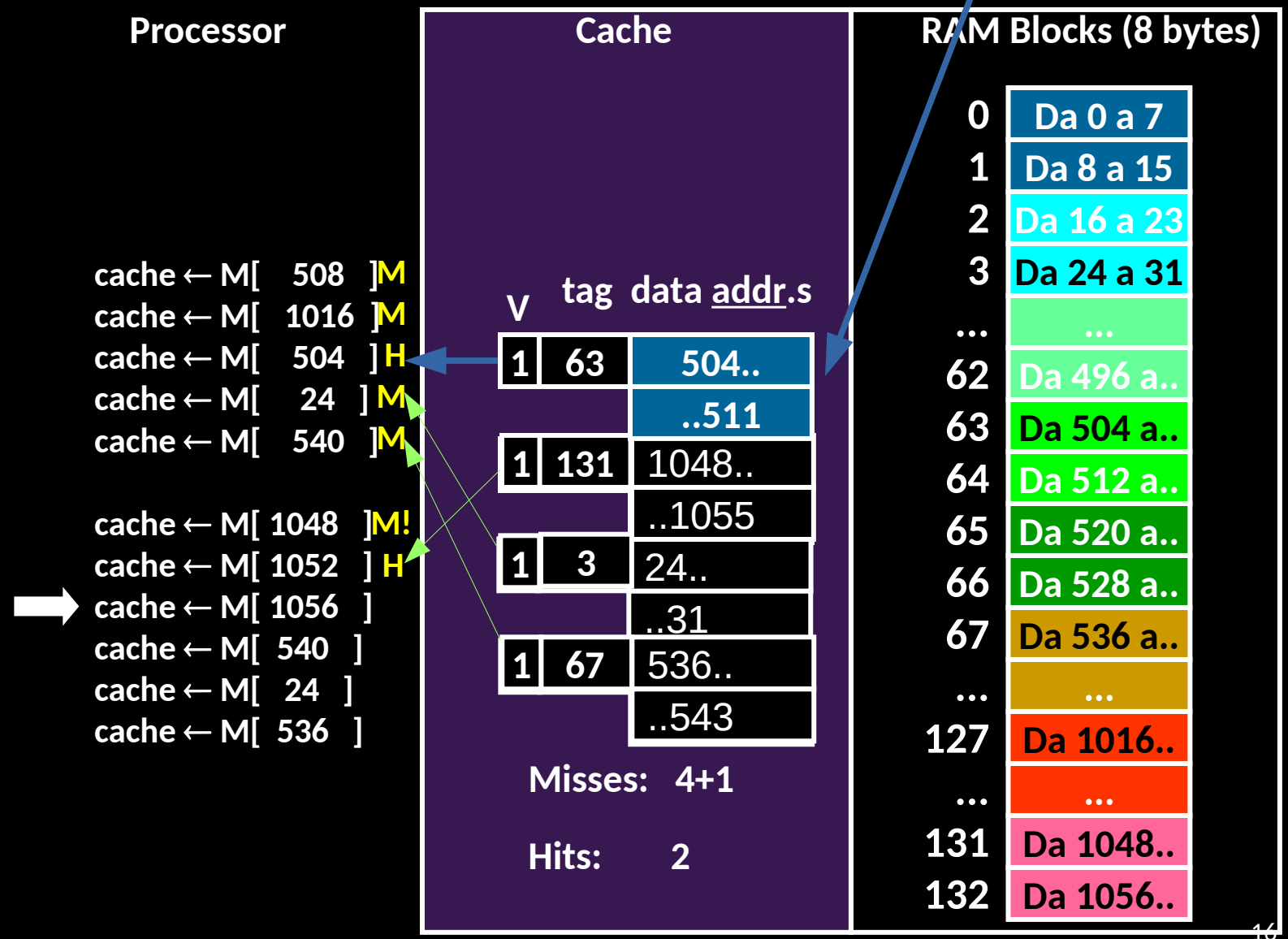

Processor
cache ← M[508]M
cache ← M[1016]M
cache ← M[504] H
cache ← M[24] M
cache ← M[540]M
cache ← M[1048]M!
cache ← M[1052]
cache ← M[1056]
cache ← M[540]
cache ← M[24]
cache ← M[536]
Cache
V tag data addr.s
1 63 504..
..511
1 131 1048..
..1055
1 3 24..
..31
1 67 536..
..543
Misses: 4+1
Hits: 1
RAM Blocks (8 bytes)
0 Da 0 a 7
1 Da 8 a 15
2 Da 16 a 23
3 Da 24 a 31
... ...
62 Da 496 a..
63 Da 504 a..
64 Da 512 a..
65 Da 520 a..
66 Da 528 a..
67 Da 536 a..
... ...
127 Da 1016..
... ...
131 Da 1048..
132 Da 1056..

A Hit

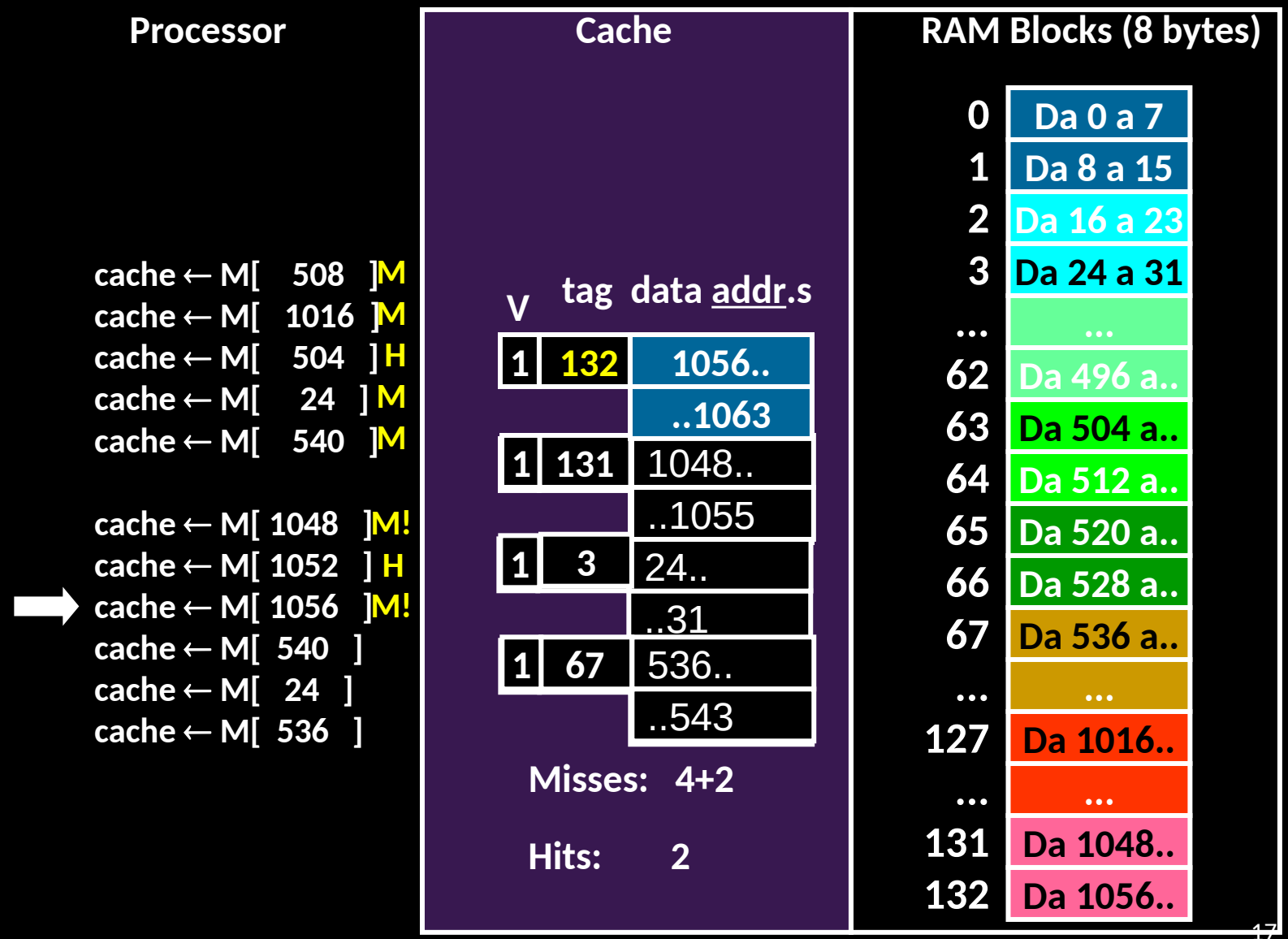

Processor
Cache
RAM Blocks (8 bytes)
cache ← M[508]M
cache ← M[1016]M
cache ← M[504] H
cache ← M[24] M
cache ← M[540]M
cache ← M[1048]M!
cache ← M[1052] H
cache ← M[1056]
cache ← M[540]
cache ← M[24]
cache ← M[536]
V
tag
data addr.s
1 63 504..
..511
1 131 1048..
..1055
1 3 24..
..31
1 67 536..
..543
Misses: 4+1
Hits: 2
0 Da 0 a 7
1 Da 8 a 15
2 Da 16 a 23
3 Da 24 a 31
... ...
62 Da 496 a..
63 Da 504 a..
64 Da 512 a..
65 Da 520 a..
66 Da 528 a..
67 Da 536 a..
... ...
127 Da 1016..
... ...
131 Da 1048..
132 Da 1056..

LRU a second time

Least recently used block in cache is:



...


Processor
cache ← M[508]M
cache ← M[1016]M
cache ← M[504] H
cache ← M[24] M
cache ← M[540]M
cache ← M[1048]M!
cache ← M[1052] H
cache ← M[1056]M!
cache ← M[540]
cache ← M[24]
cache ← M[536]
Cache
V tag data addr.s
1 132 1056..
..1063
1 131 1048..
..1055
1 3 24..
..31
1 67 536..
..543
Misses: 4+2
Hits: 2
RAM Blocks (8 bytes)
0 Da 0 a 7
1 Da 8 a 15
2 Da 16 a 23
3 Da 24 a 31
... ...
62 Da 496 a..
63 Da 504 a..
64 Da 512 a..
65 Da 520 a..
66 Da 528 a..
67 Da 536 a..
... ...
127 Da 1016..
... ...
131 Da 1048..
132 Da 1056..

Ending with 3 Hits (=> answer to exercise: total Misses=6)