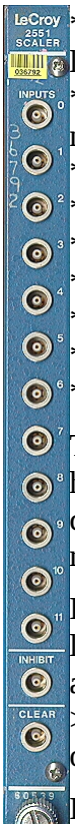
CAMAC Model 2551 12-Channel 100 MHz Scaler



* Compact packaging-12 channels per single-width module means fewer crates, smaller systems, less inhibit fan-out.
* Low cost-The high density hybrid circuit design allow common functions to serve a greater number of channels, thus lowering the cost per channel.
* Fast clear Input-Enables fast rejection of unwanted data without dataway operations.
* Less than 10 ns double-pulse resolution-1 00 MHz counting rates.
* Direct-coupled Inputs-Input sensitivity or rate capability are not dependent upon risetime.
* Input Inhibit-Common inhibit disables inputs without injecting counts.
* Test mode-Increment mode permits testing all scalers simultaneously without removing cables.
* Full LAM functions-Signals impending overflow condition.
* Full provision to cascade channels-provides > 24-bit capacity when needed.

The LRS Model 2551 contains 12 identical 24-bit binary scalers especially designed for use in high- speed nuclear counting applications. This dramatic increase in channel density over conventional 4-channel designs is made possible by state-of-the art hybrid circuits which offer reliability-enhancing low power dissipation in addition to compact packaging.

Each scaler is equipped with an extremely wideband input circuit which responds to NIM level logic signals of any duration down to 5 ns, without multiple-pulsing (in the case of wide inputs) and without counting down. The ability to recognize narrow input signals at an equivalent rate of >100 MHz is an important feature, since it assures that the scaler will accurately accumulate any output signal gener- ated by standard discriminator and logic circuits.

Each module is provided with a high-speed fast inhibit which permits simultaneous rejection of input signals at a rate equivalent to 100 MHz. The CAMAC Inhibit (1) provides inhibit control via the rear connector.The inhibit signal must overlap the input signal, but toggling the inhibit will not cause pulses to be counted.

Fast rejection of unwanted data is provided by the fast clear input. This input allows the entire scaler to be reset by application of a NIM level clear pulse without the need to perform any dataway operations.

The Model 2551 provides a full set of LAM functions. When enabled, setting of the 24th bit of any of the 12 channels is flagged by generation of LAM.

The Model 2551 has a built-in test circuit which allows all registers to be checked simultaneously. Application of the CAMAC Increment F(25) Function Code causes each scaler to advance by one count for each S2 timing signal received. The test circuit may be used without disconnecting cables if the Input or CAMAC I Inhibit is on. The 24-bit data from any scaler is read in parallel to the common dataway via the rear card-edge connector. Individual channel non-destructive readout is accomp- lished by generating a CAMAC Read F(O) and the appropriate address. Using Read and Clear F(2), the channels will be automatically zeroed after reading the last channel. Clear F(9), CAMAC Clear C, or Initialize Z will zero all channels.

The LRS Model 2551 12-Channel 100 MHz Scaler embodies refinements developed over years of experience width wideband direct-coupled discrimination and counting circuits, and, as a result, offers flexibility, reliability, and performance unmatched by any other available equipment.

SPECIFICATIONS CAMAC Model 2551 12-CHANNEL 100 MHz SCALER

Signal Input (each channel):	Threshold: > -600 mV (NIM logic levels).
Impedance:	50Ohm, direct-coupled.
Reflection:	< 10% typical at 1 ns risetime.
Protection:	+/-5 volt transients.
Minimum PulseWidth:	7 ns FWHM at -600 mV input amplitude; 5 ns FWHM at > -700 mV input amplitude.
Multiple-Pulse Resolution:	10 ns.
Counting Rate:	DC to 100 MHz.
Signal Inhibit:	Common input, -500 mV threshold, 5 ns minimum width, impedance 50 Ohm. Inhibit signal stretches internally by approx. 5 ns and must precede input signal by 10 ns. Inhibit pulses will not be counter by scaler.
Half Scale Flag:	Any scaler generates LAM when 24th bit is set.
Front-Panel Clear:	Common input, -500 mV threshold, 50 ns minimum width clears all channels with 1 us.
Capacity:	24 binary bits (1 6,777,216), (or 48 bits by cascading channels).
Cascading of Channels:	By internal wire jumper option, each even-numbered channel (i.e., 0, 2, 4, 6, 8, 1 0) may be cascaded with the subsequent odd-numbered channel to provide one 48-bit scaler. In this mode of operation, no LAM will be generated by either of the cascaded channels.
CAMAC Commands:	
C:	All scalers and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2.
Z:	Same as C, except also disables LAM.
1:	All Scaler inputs are inhibited during CAMAC "Inhibit" command.
Q:	A Q = 1 response is generated in recognition of an F(O) or F(2) Read function, or an F(8) if LAM set set for a valid N and A, but there will be no response (Q=O)

	under any other condition.
X:	An X=l (Command Accepted) response is generated when a valid F, N, and A command is generated.
L:	A Look-At-Me signal is generated from time when first 24th bit is set until a module Clear command. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM.
CAMAC Function Codes:	
F(O):	Read registers; requires N and A, A(O) through A(l 1) are used for channel addresses.
F(2):	Read registers and Clear module and LAM; requires N and A; (Clears on A(l 1) only.)
F(8):	Test Look-At-Me; requires N, and any A from A(O) to A(l 1) independent of LAM disable; Q response is generated if LAM is set.
(F(9):	Clear All scaler channels simultaneously; requires N, S2, and A from A(O) to A(l 1).
F(24):	Disable Look-At- Me; requires N, S2, and any A from A(O) to A(l 1).
F(25):	Increment all scalers; requires N, S2, and any A from A(O) to A(l 1). (inhibit should be true to prevent input pulses from being counted).
F(26):	Enable Look-At- Me; requires N, S2, and any A from A(O) to A(l 1). Remains enabled until Z or F(24).
CAUTION: The state of the LAM mark will be arbitrary after power turn-on.	
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.
Current Requirements:	+6 V at 1.2 A -6 V at 100 mA

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